Ultra Low-Noise Performance of 0.15-Micron Gate GaAs MESFET's Made by Direct Ion Implantation for Low-Cost MMIC's Applications

M. Feng, J. Laskar, J. Kruse, and R. Neidhard

Abstract— **The high-speed and noise performance of 0.15-micron gate GaAs MESFET's for microwave and millimeter-wave IC applications is reported on. The best extrinsic f_t is 109 GHz without correction for pad parasitics which is equivalent to an intrinsic f_t of 134 GHz. The 0.15 × 200-micron gate GaAs MESFET achieved 0.6-dB noise figure with 17-dB associated gain at 10 GHz and 0.9-dB noise figure with 13-dB associated gain at 18 GHz. The measured noise figure and associated gain is the best reported performance for GaAs MESFET's and comparable to the best noise/gain performance of HEMT's and P-HEMT's.**

I. Introduction

The next generation of portable communication systems such as cellular phones and radios require ultra low-noise and low-power electronics technology to support the receiver front-end. GaAs based MESFET MMIC receivers will lead to a continued reduction in the number of parts and interconnects, thereby reducing the size and weight. The receiver noise is the most important parameter which needs to be understood to improve the overall receiver system performance. The low-noise device specifications can be met by HEMT's and P-HEMT's using MBE or MOCVD technology, however, the cost, availability, reliability and manufacturability of MMIC's remains the major problems to be overcome by using epitaxial layers.

Ion implantation technology is the technology of choice in both the silicon and GaAs ICs industries due to cost-performance advantages over epitaxial technology. The first low-noise GaAs MESFET fabricated by direct ion implantation into an LEC substrate achieved a 1.3-dB noise figure with 10.3-dB associated gain at 12 GHz in 1982 [1]. Subsequently, the first 60-GHz ion-implanted GaAs MESFET and amplifier was made in 1984 [2]. However, the noise figure of ion-implanted GaAs MESFET's was not as good as to HEMT's or P-HEMT's due to the lower current gain cutoff frequency. As a result, only a few detailed noise figure performance results have been reported in GaAs MESFET's [3], [4] and MMIC's [5]. This work presents the ultra low-noise and high-speed performance of 0.15-μm × 200-μm gate GaAs MESFET's fabricated by direct ion implantation into GaAs [100] LEC substrate.

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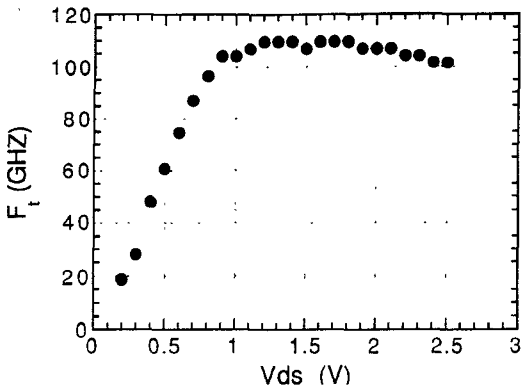

Fig. 1. Current-gain cutoff frequency f_t, as a function of V_{ds}.

II. Fabrication

The active layer was formed by two direct ion implantation of silicon ions into GaAs [100] LEC substrate in sequence. The channel implant is formed with a penetration depth of 1500Å to achieve a peak carrier concentration of 1×10^{18} cm^{-3}. The surface implant (n^+ layer) is achieved with a penetration depth of 600Å to achieve a peak carrier concentration of 2×10^{18} cm^{-3}. A capless annealing technique employing AsH_3 overpressure at 850° C was used to activate the silicon ions and the typical sheet resistance is 220 ohm/sq. E-beam direct write was used to pattern the 0.15-μm T gate. Other steps were done by using an optical shallow U.V. contact aligner. The drain-to-source spacing was 2 μm with a gate-to-source spacing of 0.5 μm to reduce the source resistance. Device isolation was achieved by mesa etching. The total gate width is 200 μm with 0.15 μm × 100 μm per finger. AuGe–Ni–Au was used for ohmic contacts and Ti–Pt–Au metalization was used for the gate channel.

III. RF Performance

The typical device showed an extrinsic transconductance

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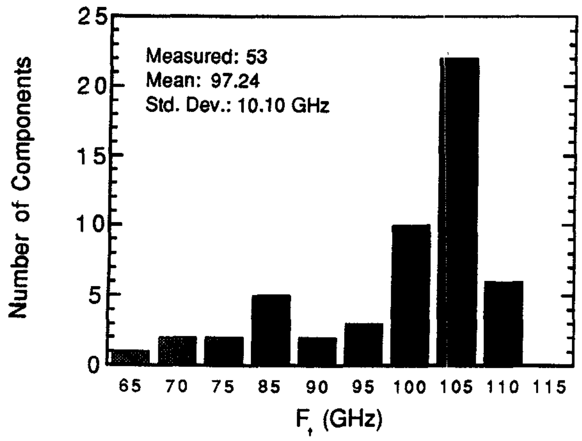


Fig. 2. Distribution of the current-gain cutoff frequency, f_t for 0.15 × 200 micron gate.

of 400 mS/mm at a drain current of I_{dss}. The current gain cutoff frequency f_t of the best device extrapolated from $|H_{21}|$ using –6 dB/octave slope, was 109 GHz without correction. This extrinsic f_t as a function of drain to source voltage (V_{ds}) is shown in Fig. 1. The f_t is related to a capacitance parameter, C_{tot}, through the equation $f_t = gm/2\pi(C_{\text{tot}})$. This capacitance, however, includes a parasitic component such as pad capacitance and due to R_d, R_s, and $R_{d}s$. A technique for accurate corrections can be made to determine the intrinsic value of f_t [6]. Hence, the corrected value of f_t is 134 GHz. The average extrinsic f_t over 50 devices from the best wafer was measured at 97 GHz as shown in Fig. 2. The average f_t for other wafers were all above 91 GHz. These results are better than the best performance GaAs HEMT's and comparable to the best performance of GaAs P-HEMT's for the same gate length where the best reported f_t data was 100 GHz for 0.15-μm gate and 110 GHz for 0.1-μm gate [7], [8].

IV. Noise Performance

The typical noise performance of the 0.15-μm × 200-μm gate GaAs MESFET's was measured using automatic testing and networking (ATN) model NP4, on-wafer automatic tuner system over the 3–18 GHz frequency range. The GaAs MESFET was biased at $I_{dss} = 98$ mA ($V_{gs} = 0$ V, $V_{ds} = 1.6$ V) first, the measured minimum noise figure and associated gain is shown in Fig. 3. The noise figure is 0.6 dB with 17-dB associated gain at 10 GHz and the noise figure increases to 0.9 dB with 13-dB associated gain at 18 GHz. We have also used Cascade Microtech noise figure test set, and found the measurement noise figure results agreed well within ±0.1 dB over the same frequency range. These noise figure results are comparable to those on AlGaAs–GaAs HEMT's. The equivalent circuit model of 0.15-μm × 200-μm GaAs FET calculated from the measured S-parameters is shown in Fig. 4.

V. Conclusion

The ultra low-noise and high-associated-gain with 0.15-μm T gate was made by direct ion implantation into GaAs LEC (100) substrates. These results demonstrate that GaAs MESFET's can achieve noise and speed performance, which is comparable to the best GaAs HEMT's and P-HEMT's.

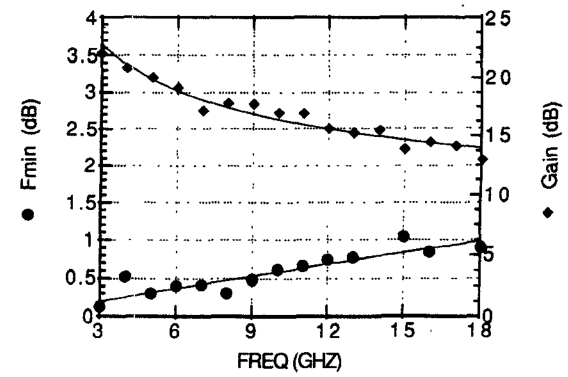
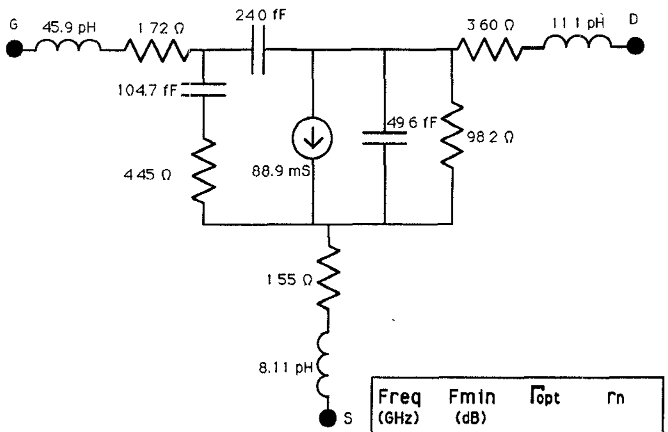


Fig. 3. Noise figure and associated gain as a function of frequency (3–18 GHz).



Freq (GHz)	Fmin (dB)	Γopt	rn
6	0.40	0.89∠23.4	1.33
12	0.70	0.83∠47.7	1.25
18	0.90	0.84∠71.0	1.06

Fig. 4. Equivalent circuit and noise parameters of the device.

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